A2

7. (Amended) A method as claimed in claim 5, wherein said causing a buffer consistency violation event comprises affecting one or both of said pointers so that the frame buffer designated by said write pointer is at least two frame buffers ahead, in said round-robin fashion, of the frame buffer designated by said read pointer.

A3

9. (Amended) A method as claimed in claim 1, further comprising determining an entering into of a state of possible frame buffer inconsistency caused by said read pointer being advanced into designating the same frame buffer as the frame buffer designated by said write pointer.

A4

13. (Amended) A method as claimed in claim 11, wherein said causing a buffer consistency violation event comprises affecting one or both of said pointers so that the frame buffer designated by said read pointer is at least two frame buffers ahead, in said round-robin fashion, of the frame buffer designated by said write pointer.

A5

15. (Amended) A method as claimed in claim 4, 7, 10, 13, 27, 28, 29, or 30, comprising generating, if said affecting is performed, a signal indicating that a frame slip has occurred.

16. (Amended) A method as claimed in claim 15, wherein said affecting of one or more of said pointers comprises affecting only said read pointer.

24. (Amended) An apparatus for transferring time slot data between ports of a switch, said apparatus comprising means for performing the method as claimed in claim 1.

A6

25. (Amended) An apparatus as claimed in claims 23, 24, or 32, comprising: N input ports and M output ports; N write pointer means of the above mentioned kind, each one being provided to operate in relation to a respective input port; N storing means of the above mentioned kind, each one being provided to temporarily store frames of time slot data received at a respective input port; N×M read pointer means of the above mentioned kind, each one being provided to operate in relation to a respective input/output port combination; and N×M control means of the above mentioned kind, each one being provided to operate in relation to a respective input/output port combination.

26. (Amended) An apparatus as claimed in claim 25, wherein said second signal is synchronized according to said first signal in such a way that: a) said second signal is permitted to show an arbitrary phase difference in relation to the said first signal; b) said second signal is permitted to show an acceptable phase jitter in relation to said first signal; and c) said second signal is not permitted to show any persistent phase drift in relation to said first signal.

Please add the following new claims 27-33:

27. (New) A method as claimed in claim 2, further comprising determining an entering into a state of possible frame buffer inconsistency caused by said write pointer being advanced into designating the same frame buffer as the frame buffer designated by said read pointer.

28. (New) A method as claimed in claim 6, wherein said causing a buffer consistency violation event comprises affecting one or both of said pointers so that the frame buffer designated by said write pointer is at least two frame buffers ahead, in said round-robin fashion, of the frame buffer designated by said read pointer.

29. (New) A method as claimed in claim 2, further comprising determining an entering into of a state of possible frame buffer inconsistency caused by said read pointer being advanced into designating the same frame buffer as the frame buffer designated by said write pointer.

30. (New) A method as claimed in claim 12, wherein said causing a buffer consistency violation event comprises affecting one or both of said pointers so that the frame buffer designated by said read pointer is at least two frame buffers ahead, in said round-robin fashion, of the frame buffer designated by said write pointer.

31. (New) A method as claimed in claim 4, 7, 10, 13, 27, 28, 29, or 30 wherein said affecting of one or more of said pointers comprises affecting only said read pointer.

32. (New) An apparatus for transferring time slot data between ports of a switch, said apparatus comprising means for performing the method as claimed in claim 17.